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For: A HIGH OUTPUT POWER QUASI-SQUARE WAVE INVERTER CIRCUIT

SECOND AMENDMENT UNDER 37 C.F.R. 312

Hon. Commissioner of Patents
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Dear Sir:

The pages relating to the claims are started on a new page as now required for scanning.

IN THE CLAIMS: Please amend the claims as follows:

1. (currently amended) A high output power inverter circuit coupled to obtain power from a voltage source (Vb) such as a battery service, the voltage source having a ground return line (Vr), the high output power inverter circuit comprising:

a toroidal transformer having a primary and a secondary winding, the primary winding having a first end, a second end and a center tap, the center tap being coupled to the voltage source,

a first and second switch to conductively couple the first end and the second end of the transformer alternately to the ground return line (Vr) during alternate half cycles of successive power cycles for respective and successive first and second on-time intervals, the toroidal transformer secondary providing a quasi-square wave output voltage ,

a pulse-width modulator and driver circuit for driving the first and second switch into conduction for each <u>first and second</u> on-time during alternate half cycles of successive power cycles, and for interposing a dead-time or non-conductive interval between the first and second on-time intervals and during the interval preceding the start of any subsequent first on-time interval,

a control circuit for sensing the on-time voltage on a non-conducting second end or non-conducting first end of the primary winding during the on-time of the respective conducting first or conducting second switch and for modulating the <u>first and second</u> on-time of the [switching means] <u>pulse-width modulator and driver circuit</u> to maintain the quasi-square wave output voltage within a predetermined range, and

an output current-voltage sensing circuit means for measuring the load current by measuring the on-time voltage on the conducting first end or second end of the primary winding with respect to the ground return line (Vr) during the on-time of the respective first or second switch, and for terminating the [switching means] <u>pulse-width modulator and driver circuit</u> <u>first and second</u> on-time in response to a predetermined on-time voltage threshold being exceeded.

2. (withdrawn) A high output power inverter from a dc voltage source having a service line providing 22 to 36 Vdc from a battery service, the source having a ground return line, the power inverter comprising:

an input transformer having a primary and a secondary winding, the primary winding having a first end and a second end and a center tap,

switching means for switching the first end and the second end of the transformer alternately to ground during alternate half cycles, a dead time or non-conductive interval being interposed between the first end and the second end of the transformer being switched to ground,

a control circuit for sensing the output voltage and for modulating the on-time of the switching means to maintain an output voltage within a predetermined range,

an acoustic reference for a clock circuit, the clock circuit controlling the start of each power cycle, and

means for monitoring the output current by measuring the reflected load current in the primary winding,

the transformer secondary having a first and second end, the first and second ends being connected to output terminals.

3. (currently amended) The high output power inverter circuit of claim 1 wherein the output current-voltage sense circuit means further comprises:

a means for measuring the load current by measuring [the] <u>a first and second</u> on-time voltage on the conducting first end or the conducting second end of the primary winding with respect to the ground return line (Vr) during the <u>first and second</u> on-time of the first [[or]] <u>and</u> second [[primary]] switch.

4. (currently amended) The high output power inverter circuit of claim 1 wherein the output current-voltage sense circuit means further comprises:

a means for measuring the load current by measuring the on-time voltage on the conducting first end or the conducting second end of the primary winding with respect to the ground return line (Vr) during the on-time of the first or second primary switch, and

a latch circuit characterized to toggle to an over-current state in response to a predetermined sensed voltage being exceeded, the over-current output state of the latch circuit providing an over-current signal to terminate the [switching means] pulse-width modulator and driver circuit first and second on-time thereby turning off the [switching means] first and second switches.

5. (currently amended) The high output power inverter circuit of claim 1 wherein the control circuit for alternately sensing the voltage on a non-conducting first end or second end of the primary winding during the on-time of the second or first [switching means] switches and for modulating the first and second on-time of the [switching means] pulse-width modulator and driver circuit to maintain an output voltage within a predetermined range further comprises:

a first and second amplifier coupled to receive, scale and filter the first and second non-conducting primary voltages to form a control voltage, the control voltage being coupled to an averaging filter to provide a filtered control voltage, the filtered control voltage being coupled to [the switching means] a pulse-width modulator and driver circuit control voltage input, the [switching means] pulse-width modulator and driver circuit modulating the first and second on-time to minimize the difference between the filtered control voltage and a reference voltage to thereby maintain the output voltage within a predetermined range.

6. (original) A high output power inverter circuit coupled to obtain power from a voltage source (Vb) such as a battery service, the voltage source having a ground return line (Vr), the high output power inverter comprising:

a toroidal transformer having a primary and a secondary winding, the primary winding having a first end and a second end and a center tap, the center tap being coupled to the voltage source,

a first and second switch to conductively couple the first end and the second end of the transformer alternately to the ground return line (Vr) during alternate half cycles of successive power cycles for respective and successive first and second on-time

intervals, the toroidal transformer secondary providing a quasi-square wave output voltage,

a pulse-width modulator and driver circuit for driving the first and second switch into conduction for each on-times during alternate half cycles of successive power cycles, and for interposing a dead-time or non-conductive interval between the first and second on-time intervals and during the interval preceding the start of any subsequent first on-time interval,

a control circuit for sensing an on-time voltage on a non-conducting second end or non-conducting first end of the primary winding during each on-time of the respective conducting first or conducting second switch and for modulating the on-time of the first and second switch to maintain the quasi-square wave output voltage within a predetermined range, and

a shunt switching circuit for connecting the first end of the primary winding to the second end to the primary winding during a dead-time between each respective on-time.

7. (currently amended) The high output power inverter circuit of claim 6 wherein the shunt switching circuit further comprises:

FET shunt switches responsive to a shunt drive signal to connect the first end of the primary winding to the second end of the primary winding during the dead-time of the first and second [switching means] switches.

8. (currently amended) The high output power inverter circuit of claim 6 wherein the control circuit further comprises:

a first and second amplifier coupled to receive, scale and filter the first and second non-conducting primary voltages to form

a control voltage, the control voltage being coupled to an averaging filter to provide a filtered control voltage, the filtered control voltage being coupled to the [switching means] pulse-width modulator and driver, the [switching means] pulse-width modulator and driver modulating the first and second on-time to minimize the difference between the filtered control voltage and

a reference voltage to thereby maintain the output voltage within the predetermined range.

9. (original) The high output power inverter circuit of claim 6 wherein the shunt switching circuit further comprises:

a dead-time detection and shunt drive circuit having a first comparator coupled to compare the amplitude of the first and second non-conducting primary voltages with a predetermined portion of the voltage source (Vb) and to output a dead-time signal in response to the non-conducting primary voltage exceeding the predetermined portion of the non-conducting primary voltage, the dead-time signal being coupled to the shunt driver circuit to command the shunt switches into the conductive state.

10. (currently amended) The high output power inverter circuit of claim 6 wherein the shunt switching circuit is further characterized to provide a shunt drive signal to first and second FET shunt switches connecting the first end of the primary winding to the second end of the primary winding during the dead-time of the first and second [switching means] switches.

11. (original) The high output power inverter circuit of claim 6 further comprising: an output current monitor circuit for measuring the output load current and for interrupting the drive signal to the shunt switching circuit when the measured output load current is below a predetermined limit to conserve operational power dissipation by interrupting shunt drive signal power during periods of very low output power.

12. (currently amended) The high output power inverter circuit of claim 6 wherein the output load current low limit detection circuit further comprises:

a [center-taped] center-tapped winding on a core having a first and second end, the first end being coupled to be in series with ground return and the first switch [means], and the second end being coupled to be in series with the ground return and the second switch [means],

a slot being cut in the core, a Hall Effect device being inserted in the slot, the Hall Effect device outputting a load-current signal,

a hall-effect amplifier being coupled to be responsive to the load-current signal for outputting a buffered and scaled load-current signal,

a comparator responsive to the load current signal for comparing the load-current signal with a predetermined reference and for outputting a shunt interrupt signal to the shunt circuit to interrupt the shunt drive signal

13. (original) The high output power inverter circuit of claim 6 further comprising:

a low battery voltage, time delay and interrupt circuit for comparing the voltage source voltage (Vb} when measured with respect to the ground return line (Vr) to a predetermined low voltage source reference voltage and for outputting a low voltage source signal in response to the voltage source voltage falling below the predetermined low voltage source voltage limit, the low voltage signal being coupled to the over-current delay and latch circuit to set the over current latch after a predetermined time delay.

14. (original) The high output power inverter circuit of claim 6 further comprising:

a high battery voltage interrupt circuit for comparing the voltage source voltage (Vb} when measured with respect to the ground return line (Vr) with a predetermined high voltage source reference voltage and for outputting a high voltage source interrupt signal in response to the voltage source voltage rising above the predetermined high voltage source voltage limit, the high voltage source signal being coupled to the over-current delay and latch circuit to set the over current latch with no predetermined time delay.

15. (currently amended) A high output power inverter circuit coupled to obtain power from a voltage source (Vb) such as a battery service, the voltage source having

a ground return line (Vr), the high output power inverter comprising:

a toroidal transformer having a primary and

a secondary winding, the primary winding having a first end and a second end and a center tap, the center tap being coupled to the voltage source,

a first and second switch to conductively couple the first end and the second end of the transformer alternately to the ground return line (Vr) during alternate half cycles of successive power cycles for respective and successive first and second on-time intervals, the toroidal transformer secondary providing a quasi-square wave output voltage,

a pulse-width modulator and driver circuit for driving the first and second switch into conduction for [[each]] <u>first and second</u> on-times during alternate half cycles of successive power cycles, and for interposing a dead-time or non-conductive interval between the first and second on-time intervals and during the interval preceding the start of any subsequent first on-time interval,

a control circuit for sensing an on-time voltage on a non-conducting second end or non-conducting first end of the primary winding during each <u>first and second</u> on-time of the respective conducting first or conducting second switch and for modulating the <u>first and second</u> on-time of the first and second switch to maintain the quasi-square wave output voltage within a predetermined range,

an output current-voltage sensing circuit means for measuring the load current by measuring [[the]] <u>a first and second</u> on-time voltage on the conducting first end or second end of the primary winding with respect to the ground return line (Vr) during the on-time of the respective first or second switch, and for terminating the [switching means] <u>first and second</u> on-time in response to a predetermined on-time voltage threshold being exceeded. and

a shunt switching circuit for connecting the first end of the primary winding to the second end to the primary winding during a dead-time between each respective on-time.

16. (currently amended) The high output power inverter circuit of claim 15 wherein the control circuit further comprises:

a first and second amplifier coupled to receive, scale and filter the first and second non-conducting primary voltages to form

a control voltage, the control voltage being coupled to an averaging filter to provide

a filtered control voltage, the filtered control voltage being coupled to the [switching means] pulse-width modulator and driver circuit, the [switching means] pulse-width modulator and driver circuit modulating the first and second on-time to minimize the difference between the filtered control voltage and

a reference voltage to thereby maintain the output voltage within the predetermined range.

17. (original) The high output power inverter circuit of claim 15 wherein the shunt switching circuit further comprises:

a dead-time detection and shunt drive circuit having a first comparator coupled to compare the amplitude of the first and second non-conducting primary voltages with a predetermined portion of the voltage source (Vb) and to output a dead-time signal in response to the non-conducting primary voltage exceeding the predetermined portion of the non-conducting primary voltage, the dead-time signal being coupled to the shunt driver circuit to command the shunt switches into the conductive state.

18. (currently amended) The high output power inverter circuit of claim 15 [wherein the] further comprising:

an output load current low limit detection circuit having [further comprises:]

a [center-taped] center-tapped winding on

a core, the center-tapped winding having a first and second end, the first end being coupled to be in series with ground return and the first switch [means], and the second end being coupled to be in series with the ground return and the second switch [means], a slot being cut in the core, a Hall Effect device being inserted in the slot, the Hall Effect device outputting a load-current signal,

a hall-effect amplifier being coupled to be responsive to the load-current signal for outputting a buffered and scaled load-current signal, a comparator responsive to the load current signal for comparing the load-current signal with a predetermined reference

and for outputting a shunt interrupt signal to the shunt circuit to interrupt the shunt drive signal.

19. (original) The high output power inverter circuit of claim 15 further comprising:

a low battery voltage, time delay and interrupt circuit for comparing the voltage source voltage (Vb} when measured respect to the ground return line (Vr) with a predetermined low voltage source reference voltage and for outputting a low voltage source signal in response to the voltage source voltage falling below the predetermined low voltage source voltage limit, the low voltage signal being coupled to the over-current delay and latch circuit to set the over current latch after a predetermined time delay

20. (original) The high output power inverter circuit of claim 15 further comprising:
a high battery voltage interrupt circuit for comparing the voltage source voltage (Vb} when measured respect to the ground return line (Vr) with a predetermined high voltage source reference voltage and for outputting a high voltage source interrupt signal in response to the voltage source voltage rising above the predetermined high voltage source voltage limit, the high voltage source signal being coupled to the over-current delay and latch circuit to set the over current latch with no predetermined time delay.